APPLICATION NOTE

TJA 1010
Octal Low Side Driver (OLSD)

AN98057

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Abstract

The Octal Low Side Driver TJA1010 is a smart power device, dedicated for controlling up to eight relays. It is designed to operate under the harsh environmental conditions in an automotive system. For example, it handles the wide voltage range, that can occur in a vehicle´s supply network and its output stages are fully protected. The TJA1010 can be controlled by a microcontroller via a serial peripheral interface (SPI). Via the SPI also full diagnostic information from the load outputs is delivered. Further features are two status outputs, low-power mode, power-on reset, over- and undervoltage shutdown.

This application note gives information on the implementation of the TJA1010 into an electronic control unit, focusing on the requirements of automotive systems.

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APPLICATION NOTE

TJA 1010
Octal Low Side Driver (OLSD)

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Summary

This application note is intended to provide application support for designing the TJA1010 into electronic control units, especially in automotive systems.

The paper discusses the interface of the device to the loads, the microcontroller and the supply. Therefore, the characteristics and features of the output stages are described, including a thermal model. The device behaviour under typical supply network conditions in a vehicle is covered. Furthermore, control and diagnostics with a microcontroller are described in detail.

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1. INTRODUCTION

The Octal Low Side Driver TJA1010 contains eight DMOS switches, which are dedicated to drive relays in a car. Figure 1 shows, how the TJA1010 is typically implemented into an electronic control unit (ECU). The switches are in low side configuration. Thus they switch one load terminal to ground, while the other load terminal is permanently connected to the supply. Control of the switches is performed by a microcontroller via a serial interface (Serial Peripheral Interface = SPI). Besides the pure switching function, the TJA1010 also provides diagnostic functions: Faults at its load outputs (open load or short circuit load) are detected and signalled by means of two status outputs. Furthermore, fault information can be read by the microcontroller via the SPI, which allows to localize a fault. The TJA1010 is designed to withstand the harsh conditions in an automotive system. This is covered by wide temperature and supply voltage ranges as well as protection features.

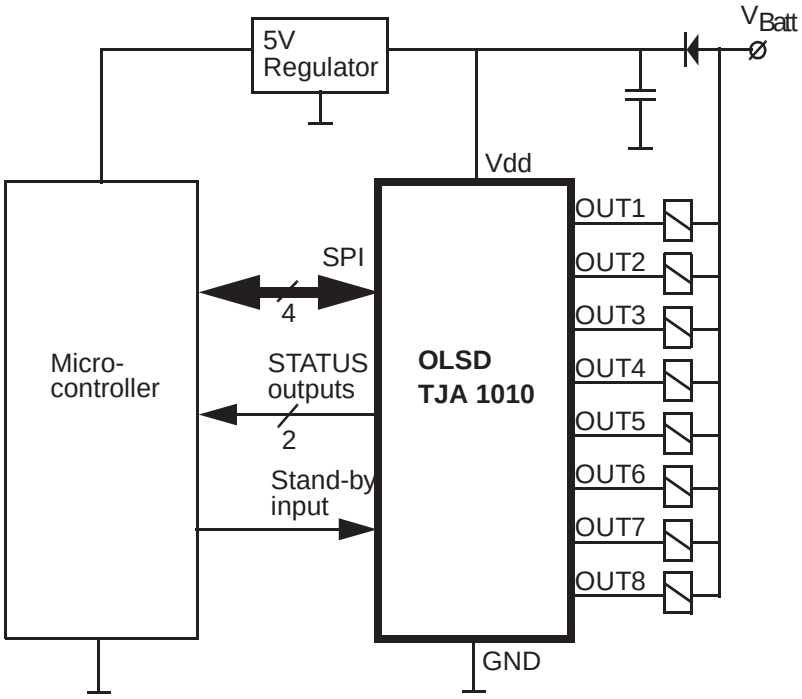

Fig. 1 Implementation of the Octal Low Side Driver into an automotive ECU

The intention of this Application Note - together with the data sheet of the device [1] - is to provide the information, which the designer needs for a successful implementation of the TJA1010 into his ECU.

2. FEATURES

Figure 2 shows a simplified block diagram of the TJA1010.

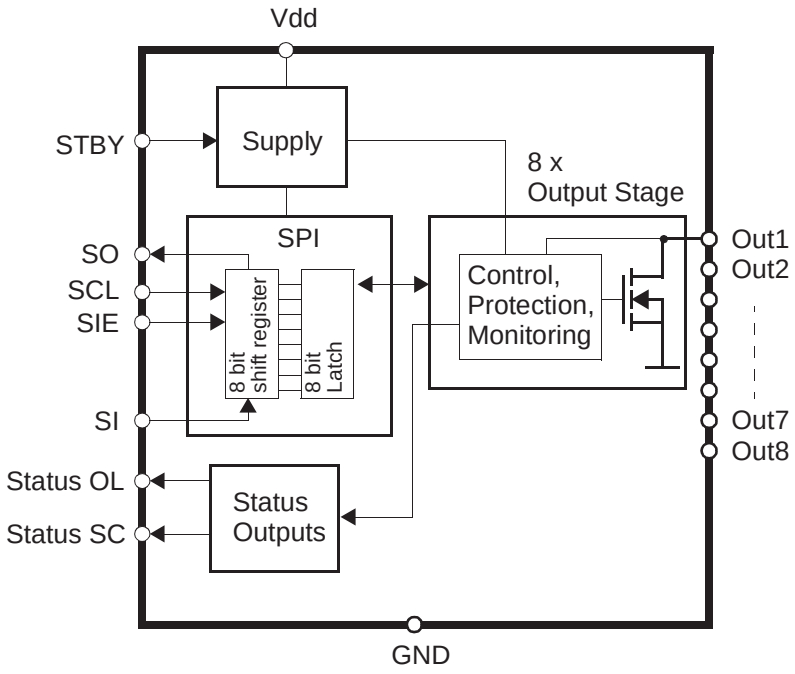

Fig. 2 Simplified block diagram

The overall circuit can be subdivided into four blocks. These blocks and their features are listed below:

- 8 Output stages
  - Independent DMOS low side drivers
  - Over voltage clamping
  - Protection against short circuit load and overload
  - Load dump protection
- Supply interface
  - Wide operating voltage range, allowing direct supply from 12 V line in a car
  - Low-power mode for minimum current consumption
  - Undervoltage shutdown / power-on reset
- Serial Peripheral Interface (SPI)
  - Control of output stages by writing data into internal shift register (SPI)
  - Channel selective diagnostic information available by reading data from internal shift register
  - Serial output (SO) allows cascading of several OLSDs
- Status outputs
  - Indication of short circuit load (STATSC) or open load (STATOL) at any output stage.

Table 1 summarizes the pin functions of the TJA1010:

Pin	Function
Vdd	Supply
GND	Ground
OUT1...8	Load outputs 1...8
STBY	Stand-by input
SI	Serial input
SO	Serial output
SCL	Serial clock
SIE	Serial input enable
STATSC	Status output, short circuit
STATOL	Status output, open load

Table 1 Pin functions

3. OUTPUT STAGES

The block diagram in fig. 3 shows a detailed view on an output stage of the TJA1010. The output stages are controlled by the SPI interface. The power switches are realized as DMOS transistors. Each stage contains circuits for driving and protection of the DMOS. Also the circuit for detecting short circuit and open load faults at the output are included here. The signals derived by this detector are partly used within the output stage for short circuit protection. Besides that, signals from here are fed to the SPI and to the status outputs for diagnostic purposes, as described in section 6.1.

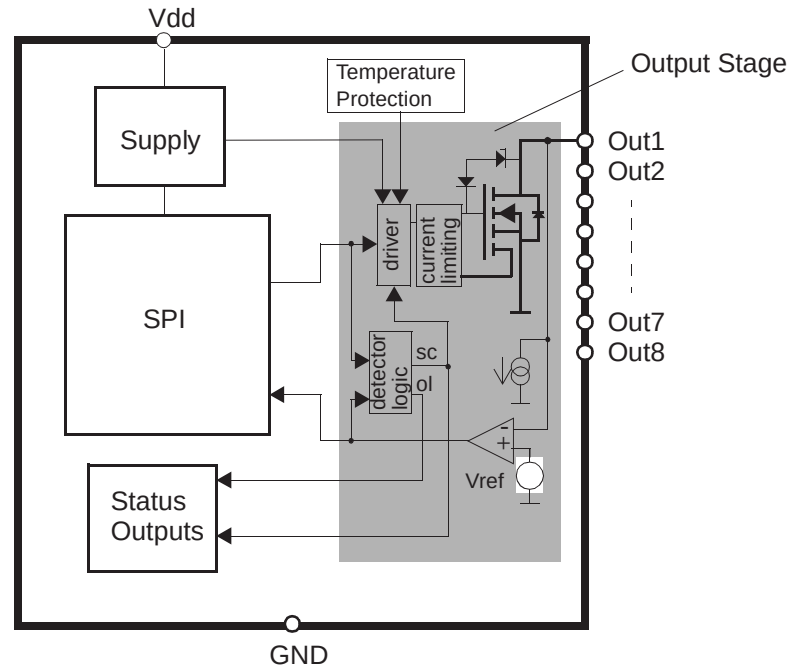

Fig. 3 Block diagram with detailed view on output stage

3.1 DMOS Power Switches

3.1.1 General Characteristics

The output drivers of the TJA1010 are DMOS (double diffused MOS) transistors with an on-state resistance of max. 3 Ω under normal supply conditions in a car. DMOS technology has been chosen because of its typical advantages over bipolar transistors:

- Almost zero power dissipation for gate drive
- No second breakdown, thus higher ruggedness in case of overvoltage
- Paralleling of output transistors is possible with thermal longtime stability.

3.1.2 Maximum Load Current / Thermal Management

Each output of the TJA1010 can be operated with a continuous current of max. 200 mA, if its junction temperature does not exceed 135 °C. If the junction temperature is even held at or below 95 °C, the max. continuous output current is 300 mA. Above 300 mA, current limiting becomes active.

The thermal model in fig. 4 supports calculation of junction temperature T_j in the output transistors: The TJA1010 comes in an SO “medium power” package with 8 GND-pins (pins 6...9 and 20...23), which are part of the leadframe. Thus, thermal paths in fig. 4 lead from the junctions of the DMOS outputs via a ´heat accumulation point´ in the chip to these GND-pins and from there to ambient. This gives a significantly lower thermal resistance as for standard SO packages, where heat is mainly radiated from the plastic package to the ambient.

The thermal resistance from GND-pins to ambient is determined by the board, on which the device is mounted. The value given here is valid for the simplest board with minimum footprint. It can be reduced e.g. by using a GND pad in order to improve heat radiation from board to ambient. A GND pad in the order of 6 cm^2 reduces the thermal resistance by 10...15 K/W.

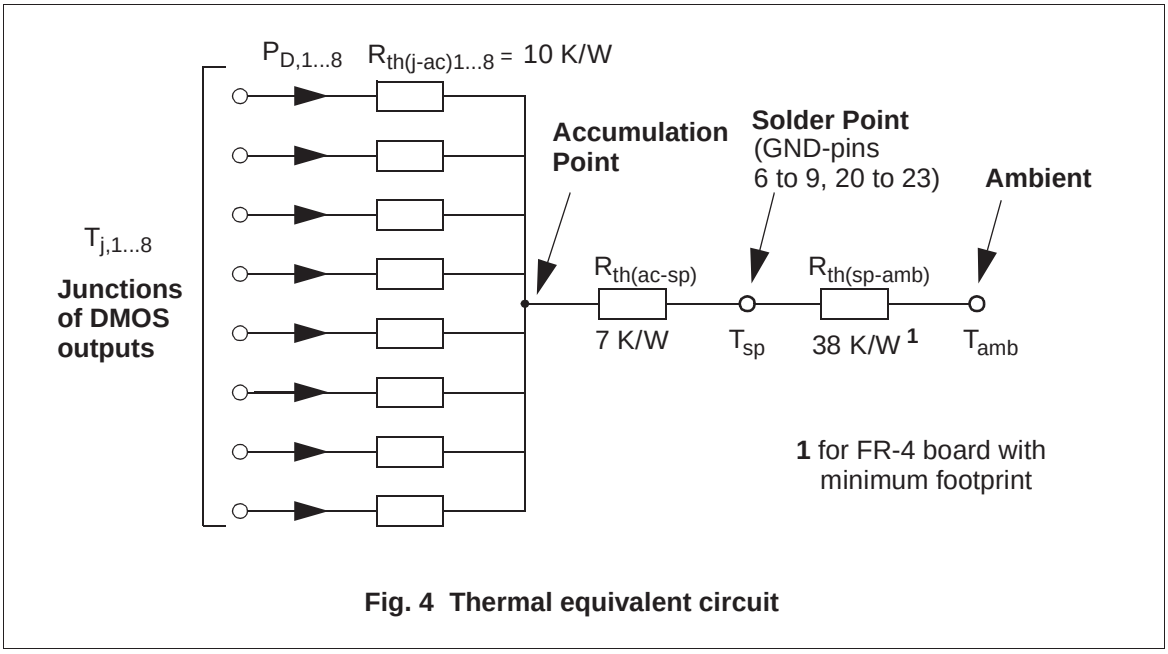

Fig. 4 Thermal equivalent circuit

Table 2 summarizes the description, the values and the electrical analogies of the thermal parameters in figure 4.

Parameter in figure 4	Description	Value	Electrical analogy
$P_{D,1...8}$	Power dissipation in output 1...8	See table 3	Current
$T_{j,1...8}$	Junction temperature in output 1...8	See table 3; max. 135 °C for continuous operation	Potential, i.e. ΔT is analog to voltage
T_{sp}	Solder point temperature (GND-pins 6...9 and 20...23)		
T_{amb}	Ambient temperature	Application dependant	
$R_{th(j-ac),1...8}$	Thermal resistance from junction of output 1...8 to "heat accumulation point"	10 K/W	Resistance
$R_{th(ac-sp)}$	Thermal resistance from "heat accumulation point" to solder point of Ground pins (pins 6...9, 20...23)	7 K/W	
$R_{th(sp-amb)}$	Thermal resistance from solder point to ambient	≤ 38 K/W, dependent on board	

Table 2 Thermal parameters and their electrical analogies

Table 3 gives equations for power dissipation, junction temperature and maximum permissible output currents, based on the thermal model of fig. 4. Equation (2) is derived by using the electrical equivalents in table 3 and applying Ohm´s law. Equations (3), (4) give the permissible dissipation and output current respectively, derived from (1) and (2), if the junction temperature should not exceed a value of $T_{j(max)}$. The continuous output current should not exceed the values stated below (4), even if (4) yields a higher value. All equations given here are valid for equal dissipation in all outputs. Fig. 4 however allows to derive equations also for any other load condition.

Quantity	Equation for equal dissipation in all outputs
Dissipation in one output	$P_D = I_{out}^2 \cdot R_{out} = I_{out}^2 \cdot 3\Omega$ (1)
Output junction temperature	$T_j = T_{amb} + P_D (R_{th(j-ac)} + 8 (R_{th(ac-sp)} + R_{th(sp-amb)}))$ (2)
Maximum permissible dissipation in one output	$P_{D(max)} = \frac{T_{j(max)} - T_{amb(max)}}{R_{th(j-ac)} + 8 (R_{th(ac-sp)} + R_{th(sp-amb)})}$ (3)
Maximum permissible current in one output	$I_{out(max)}$ = Minimum of: $\sqrt{\frac{T_{j(max)} - T_{amb(max)}}{R_{out} (R_{th(j-ac)} + 8 (R_{th(ac-sp)} + R_{th(sp-amb)}))}}$ (4) and 200 mA @ $T_{j(max)}$ = 135 °C or 300 mA @ $T_{j(max)}$ = 95 °C

Table 3 Thermal equations

Calculation Example

The maximum permissible current per output stage is to be calculated, if the TJA1010 is mounted on an FR-4 board with minimum footprint. All outputs are connected to an identical load. The maximum ambient temperature is 85 °C:

Equation (4) yields a maximum current of $\sqrt{\frac{(135-85)\,°C}{3\Omega \cdot (10+8\cdot(7+38))\,(K/W)}} = 0,21A$, if the OLSD will be operated at its temperature rating of 135 °C. Thus each output can be operated up to its current rating of 200 mA.

According to equation (1), the power dissipation per output then is: $P_{D(max)} = (0,2A)^2 \cdot 3\Omega = 0,12W$, leading to a permissible total power dissipation of $P_{D,tot(max)} = 8 \cdot 0,12W \approx 1W$.

3.2 Protection Features

3.2.1 Overvoltage Clamp

The TJA1010 is protected against overvoltage pulses at its output pins by means of clamp circuits, as shown in figure 3: The zener diode between drain and gate of each output transistor will turn that transistor partially on, if its output voltage exceeds a level of 50 V. By this means, the output voltage is clamped at a level of typically 60 V. This is below the breakdown voltage of the DMOS drivers and all other parts within the TJA1010, which are connected to the output pins.

In automotive applications, there are two possible sources for overvoltage at the output pins, that could activate the output clamps:

- Positive voltage transients on the supply line, according to ISO 7637 (see section 4.2)
- Turn-off of an inductive load without freewheel diode (see section 3.3)

3.2.2 Short Circuit and Overload Protection

The OLSD is protected against short circuit load and overload by a combination of current limiting and a 2-stage over temperature protection:

- The output current in the TJA1010 is limited to max. 550 mA. By this means, the power dissipation and thus the rate of temperature rise in the device is limited.
- If the chip temperature exceeds the “overtemperature control” threshold of typically 170 °C, the first stage of the temperature protection turns off those outputs, where a short circuit condition has been detected, i.e. where the output voltage is above a reference V_{ref} of max. 1.9 V (see fig. 3).
- Overload or “soft short circuit” conditions could exist, which do not raise the output voltage above V_{ref}. Outputs operating under such conditions would not be turned off at the first stage of the temperature protection. If such overloads would cause the chip temperature to exceed the “emergency temperature shutdown” threshold of typically 190 °C, the second temperature protection stage will turn off all outputs of the OLSD.

At both temperature protection stages, the respective outputs are turned off only for the duration of the over temperature condition. They turn on again automatically, if the chip temperature has fallen below the overtemperature control threshold.

Although the over temperature protection prevents device failure at short circuit or overload, operating the device at such high temperatures over a long time will reduce its reliability. Thus it is recommended, to turn those outputs permanently off, where short circuit or overload has been detected (see section 6).

3.3 Driving Relays

The TJA1010 is suitable for driving inductive loads like relay coils. At turn-off, the inductive energy stored in a coil has to be removed. This can principally be done by a freewheel diode across the coil. The TJA1010 however allows to save this extra component, as its DMOS output transistors are clamped. Figure 5 shows typical waveforms of output voltage and output current at the TJA1010, when turning off an inductor without freewheel diode. The kickback voltage at the load output, generated by the inductive coil energy, is clamped by the TJA1010 to a safe value of typically 60 V.

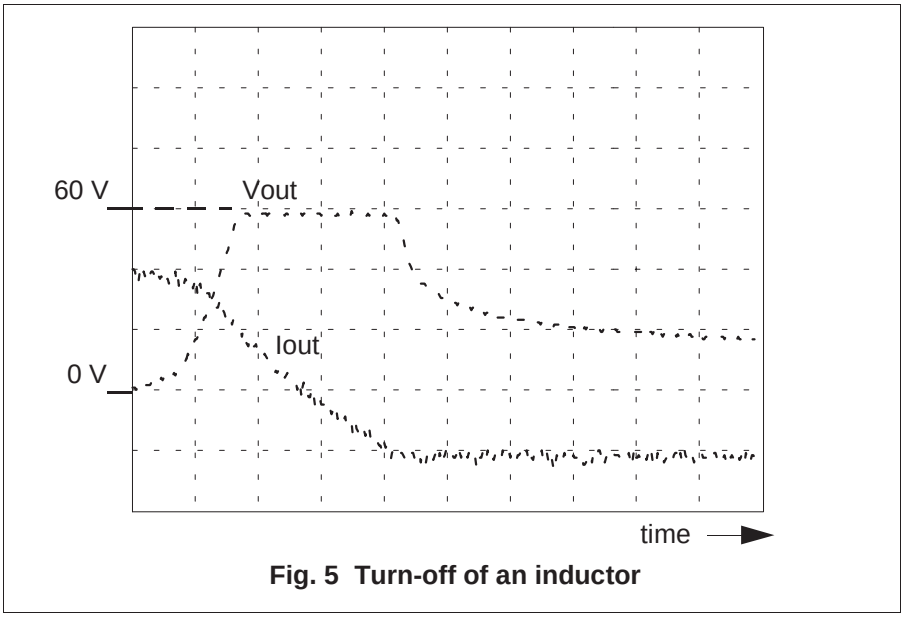

Fig. 5 Turn-off of an inductor

During clamping, power dissipation and thus a rise of junction temperature occurs in the OLSD outputs. A waveform for maximum current vs. time during inductive turn-off is given in the datasheet ([1], fig. 5). If the acutal I_{out} vs. time during clamping does not significantly exceed this waveform, the junction temperature will stay within safe limits. This is valid, even if the junction temperature at turn-off is at its dc rating of 135 °C and all eight outputs are turned off simultaneously.

The maximum current waveform in the data sheet gives a safe limit, that can be stated after tests carried out so far. The results of further tests may allow to extend that limit, permitting clamping at higher coil currents and/or longer time. Information on this subject will be available on request.

4. SUPPLY INTERFACE

4.1 Behaviour under Typical Supply Conditions in a Car

The TJA1010 is designed to handle the wide voltage range, that can occur in the supply network of a car. Table 4 summarizes the typical voltage levels in a 12 V car supply system and the respective behaviour of the TJA1010.

Typical Voltage Range [V]	Supply Condition	TJA1010 Behaviour
> 50	Positive transients (ISO 7637)	External protection required at Vdd - Pin; Outputs are internally clamped at 60 V, but energy rating to be considered.
25 to 50	Clamped load dump	Shutdown of all output stages above 25 V, where $V_{out} > V_{ref}$, see section 4.2.
16 to 25	Jump start or regulator degraded	Normal operation
10.5 to 16	Normal	
6 to 10.5	Starting phase or regulator degraded	
0 to 6	Starting phase (diesel)	Undervoltage shutdown, i.e. supply circuit shuts down all output stages below 4.3 V.
< 0	Negative transients (ISO 7637), reverse battery	External blocking diode required, see section 4.2.

Table 4 TJA1010 behaviour versus supply conditions

4.2 Supply Transients (ISO 7637) and Clamped Load Dump

Figure 6 shows a circuit for protecting the TJA1010 against positive and negative transients on the supply line. According to table 4, the TJA1010 requires external protection at its supply pin against positive voltages >50 V and against negative voltages. This is provided by ZD1 and D1 respectively. D1 also serves as reverse battery protection and is required in most ECUs anyway in order to protect the 5V-regulator, as indicated in figure 6. The function of C1 is to supply the OLSD and other components connected to V_{Batt} during negative transients, where D1 is blocking. C2 should provide a low impedance to GND for transients with high dV/dt.

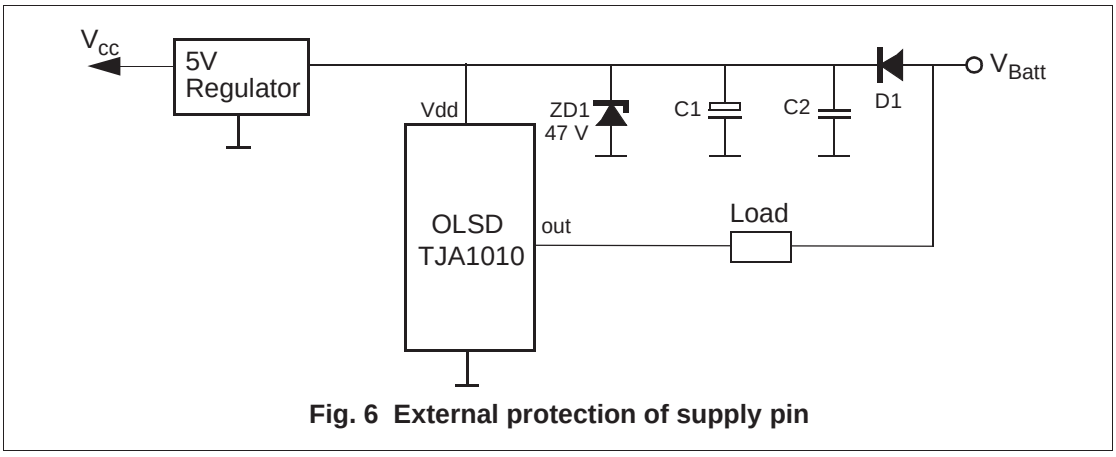

Fig. 6 External protection of supply pin

Table 5 summarizes the TJA1010 behaviour with the protection circuit in figure 6, when applying the most commonly required test pulses for a 12 V vehicle supply system.

	Pulse 1 (ISO 7637)	**Pulse 2 (ISO 7637)**	**Pulses 3a/3b (ISO 7637)**	**Clamped Load Dump**
Pulse parameters	Vs = -100 V Ri = 10 Ω td = 2 ms t2 = 200 ms	Vs = 100 V Ri = 10 Ω td = 0.05 ms t2 = 200 ms	Vs = -150/+100V Ri = 50 Ω td = 0.1 µs	V_{Batt} = 50 V for 500 ms
TJA1010 behaviour during pulse	Vdd pin only supplied by C1! Undervoltage shutdown, i.e. all outputs off, if Vdd falls below 4.3 V. Otherwise operation unaffected.	Overvoltage shutdown, i.e. all outputs off, as long as Vdd > 25 V	Operation unaffected	Overvoltage shutdown, i.e. all outputs off, as long as Vdd > 25 V
TJA1010 functional status after pulse	After shutdown: All outputs off, i.e desired output states to be restored via SPI	Unchanged, i.e. as prior to the pulse		
	Otherwise:			

Table 5 TJA1010 behaviour with supply line transients (protection circuit of figure 6 connected)

5. SERIAL PERIPHERAL INTERFACE (SPI)

Using a serial instead of a parallel interface, allows to control all 8 output stages with only 3 instead of 8 pins (serial input, clock and serial enable). By adding a further pin (serial output), it is possible to read channel selective status information with only 4 instead of 16 pins. Beyond that, a serial interface allows cascading in order to drive several OLSDs without spending further microcontroller pins.

The Serial Peripheral Interface or SPI has become an industry standard for serial synchronous interfaces between microcontrollers and “slave devices” like smart power ICs. Many microcontrollers are nowadays available with a hardware implementation of SPI, thus minimizing the software effort to drive this type of interface. However, for all other microcontroller types, SPI can still be emulated by software.

5.1 Data Transfer between TJA1010 and Microcontroller

The block diagram of figure 7 shows, that the SPI basically consists of a ring register structure. The ring register is built of two 8-bit shift registers, one implemented into the microcontroller and the other one into the “slave device”, here the OLSD. There are four interface signals: two data signals and two control signals. The latter are provided by the microcontroller and consist of a clock signal, linked with both shift registers and an enable signal for the OLSD. In a microcontroller with implemented SPI, the clock signal is generated by the SPI unit. The enable signal has to be provided by a standard I/O port pin.

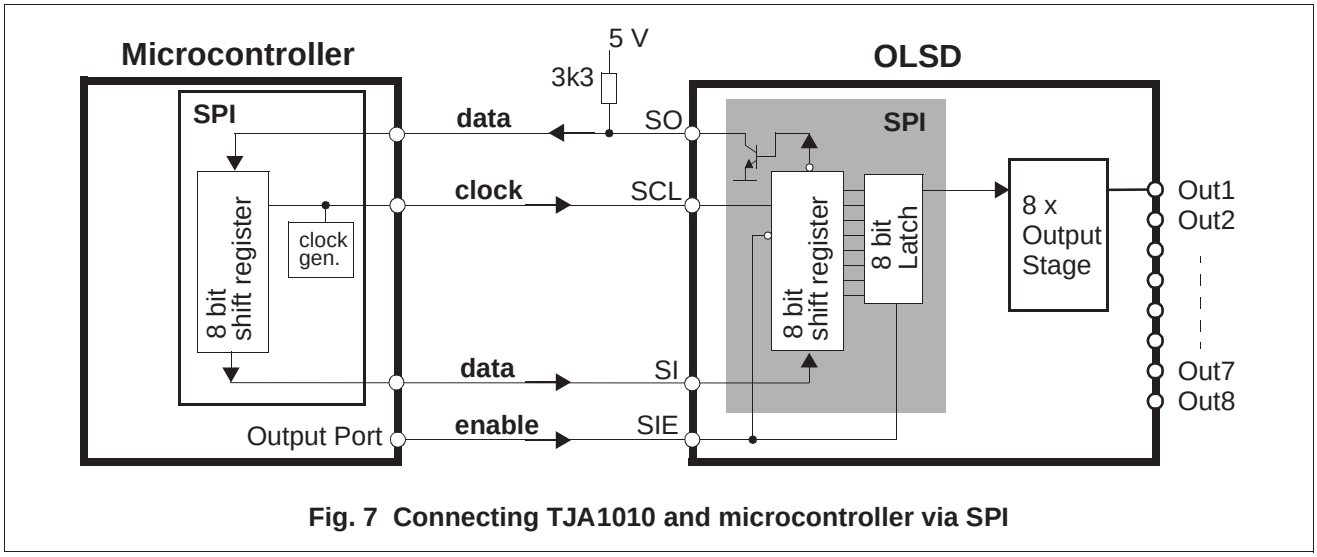

Fig. 7 Connecting TJA1010 and microcontroller via SPI

Table 6 lists the SPI pins of the TJA1010 and their functions. It also shows the pin names, which are commonly used for the respective microcontroller pin, if the latter has an implemented SPI.

Figure 8 shows the signals at the SPI pins of a TJA1010, recorded during a byte transfer. The microcontroller initiates the transfer by applying a low-level to the SIE pin. This enables the TJA1010´s shift register to serial input/output operation. Then 8 clock cycles are generated by the microcontroller. Bits are shifted by both shift registers on each low-to-high transient of the clock signal. Thus after the 8th clock cycle, both shift registers have exchanged their data. The transfer is finished, when the microcontroller applies a high-level to the SIE pin. This disables the TJA1010´s serial input/output and enables parallel loading of the new data into the 8-bit latch, which controls the output stages. Bits 1 to 8 received at the SI pin during the transfer, control output stages out1 to out8 respectively. A high-level turns an output stage on. Thus the data received at SI in fig. 8 indicate, that output stages 1,3,5,7 go off and output stages 2,4,6,8 go on at the end of the transfer.

TJA1010			MICROCONTROLLER
Pin	**Description**	**Pin Characteristic**	**Respective pin**
SI	**Serial Input** data input for control, high-level = output stage on	CMOS input	Serial Output
SO	**Serial Output** for cascading and diagnostics (sections 5.3 and 6)	open collector	Serial Input
SCL	**Serial Clock Input** shift at each low-to-high transient	CMOS input	Clock Output
SIE	**Serial Input Enable** = low-level during SPI data transfer	CMOS input	Output Port

Table 6 SPI pins of the TJA1010

The byte shifted out at the SO output is normally identical to that byte, which has been sent to the OLSD during the previous transfer. If however a fault at one of the TJA1010´s outputs has been detected after that previous transfer, the bit corresponding to the faulty output stage appears inverted at SO. Thus, a channel selective diagnostic can be carried out by comparing the received byte at SO with the byte, previously sent to SI. Section 6 describes this in more detail. The waveforms of fig. 8 have been recorded while repetitively transferring the same byte to the OLSD. The data at SI and SO are identical here, thus no fault has been detected.

The SO output can also be used for cascading of several OLSDs. This is described in section 5.3.

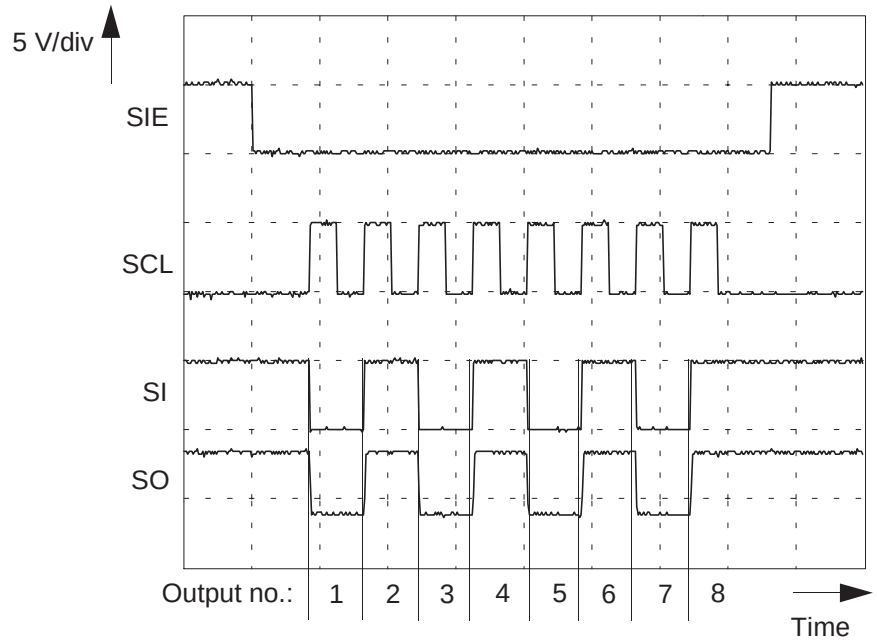

Fig. 8 SPI signals during byte transfer

5.2 Controlling the TJA1010 with a Microcontroller

Fig. 9 shows an instruction sequence for a microcontroller with implemented SPI, that will transfer a control byte to an OLSD. Prior to any data transfer, the microcontroller´s SPI system has to be initialized for the operating modes, required for the TJA1010. Each data transfer has to be started by setting that I/O port to logic 0, which is connected to SIE at the TJA1010, enabling its shift register for serial transfer. After writing the control byte for the OLSD into the SPI data register, the SPI circuit automatically generates 8 clock cycles at its clock output. Bits are now shifted out of the microcontroller´s serial output pin and out of the TJA1010´s SO pin, until both shift registers have exchanged their data. The end of the byte transfer, i.e. the end of the 8th clock cycle is indicated within the microcontroller by a dedicated flag. When setting SIE to logic 1, serial transfer at the TJA1010 is disabled and the new shift register data are loaded into the 8 bit latch, to control the output stages.

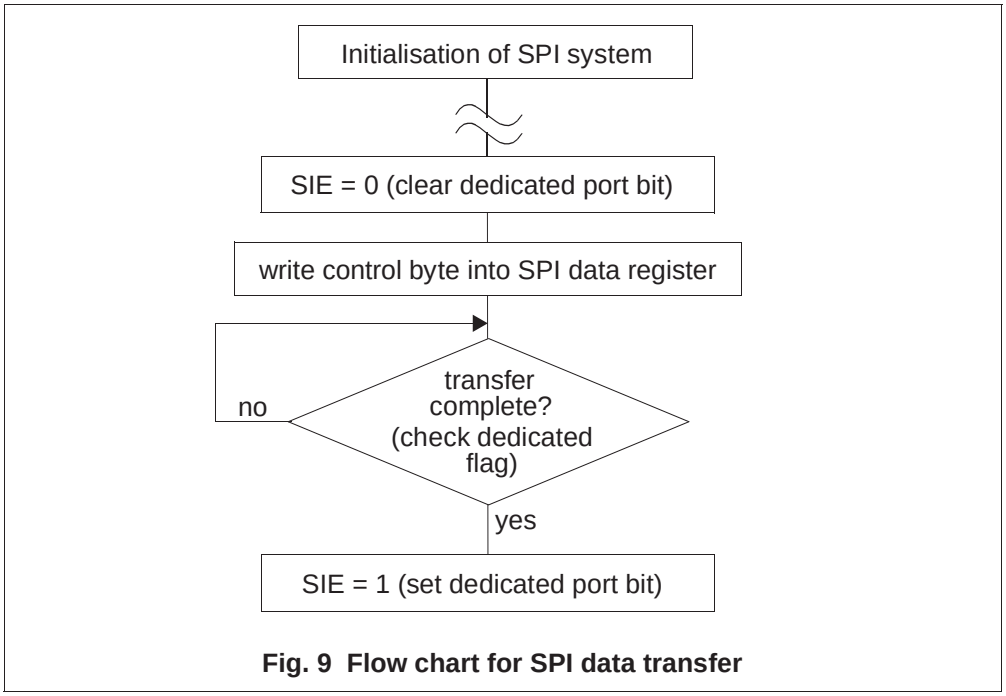

Fig. 9 Flow chart for SPI data transfer

5.3 Cascading of OLSDs (Daisy Chain)

In applications, where more than eight relays have to be controlled, SPI allows the cascading of OLSDs to form a daisy chain, as shown in fig. 10. Here, the serial inputs SI and outputs SO of n OLSDs are connected to build a shift register with n bytes. The clock signal and the enable signal are fed to the SCL and SIE pins of all OLSDs in parallel. Thus not more than four microcontroller pins are necessary to drive a principally unlimited number of OLSDs.

Fig. 11 shows the SPI waveforms in such a daisy chain, consisting of n OLSDs. Basically, the whole SPI data transfer between a microcontroller and such a daisy chain consists of n single byte transfers. Each single byte transfer functions as already described in sections 5.1 and 5.2. The first byte is for OLSD n and the last byte is for OLSD 1. Before the last byte has been transferred, each OLSD shift register contains control data, which are not dedicated for that device. Thus it has to be made sure, that the shift register data cannot affect the output stages, before the last byte has been transmitted. Therefore, the SIE pins of all OLSDs in the chain have to be kept permanently at low-level, until the last byte has been transferred.

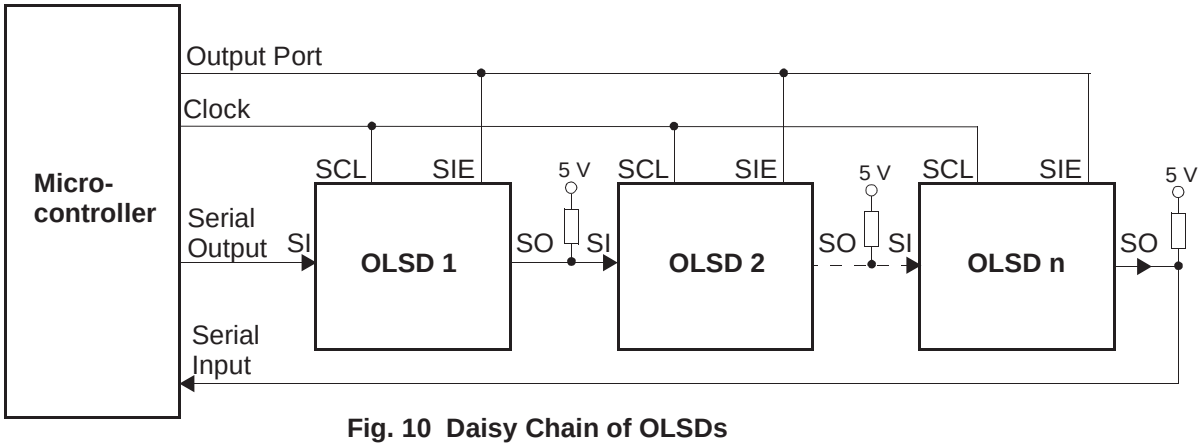

Fig. 10 Daisy Chain of OLSDs

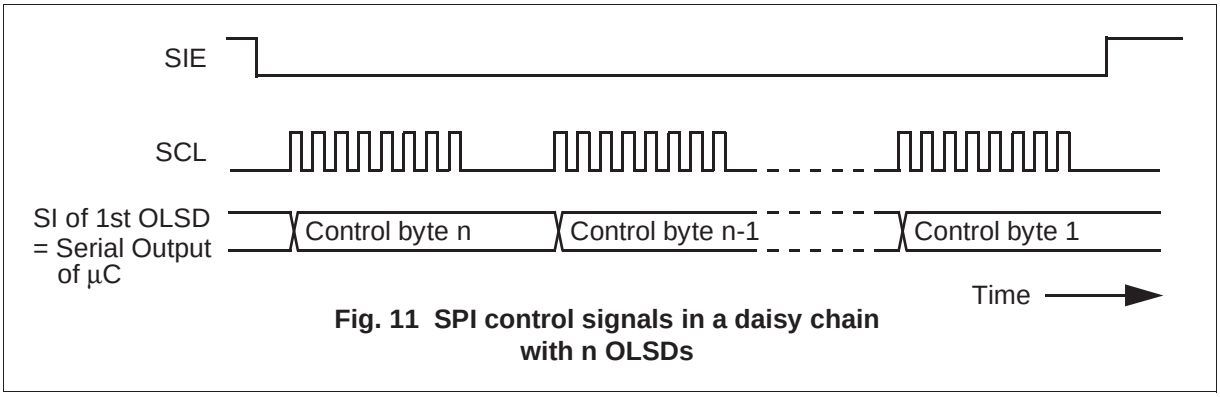

Fig. 11 SPI control signals in a daisy chain with n OLSDs

6. DIAGNOSTICS

The TJA1010 provides diagnostic information about the loads, which are connected to its output stages. Faults like “open load” (i.e. faulty connector, broken cable) and “short circuit” (i.e. load shorted) are detected and reported to the microcontroller. The following sections describe, how faults are detected and signalled by the device and how to evaluate these signals with a microcontroller.

6.1 Diagnostic Functions of the TJA1010

The block diagram of fig. 12 shows the diagnostic functions of the TJA1010. Each output stage monitors the load output voltage in order to detect open loads or short circuit loads. If such a fault has been detected, it is signalled to the shift register and to the respective status output.

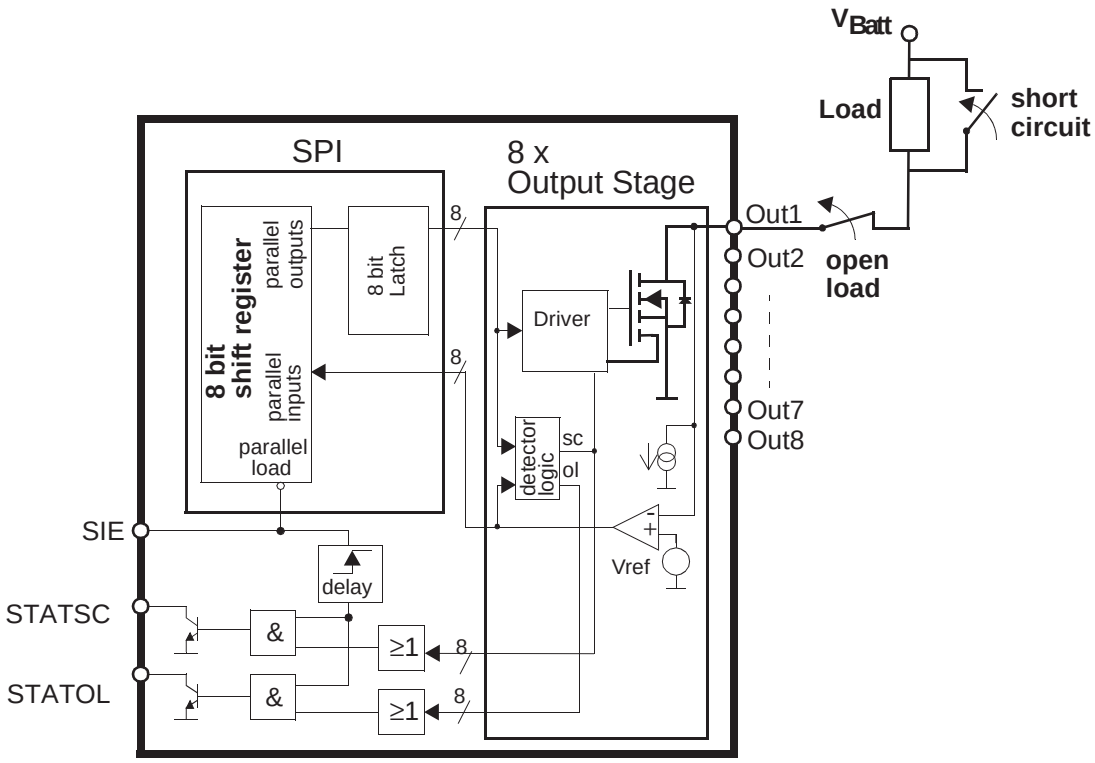

Fig. 12 Diagnostic functions

The detector circuit compares the output voltage with a reference voltage Vref. By this means, an open load is detected, if the output voltage is below Vref in off-state. A pull-down current source at each output provides a defined low output voltage in case of open load. A short circuit load is detected, if the output voltage is above Vref in on-state. “Soft” short circuit load or overload conditions, that don’t force the output voltage above Vref in on-state will be detected, if emergency temperature shutdown occurs to protect the device. In that case, the output voltage will also exceed Vref (see also section 3.2.2).

The comparator output of each output stage is linked with a parallel input of the shift register. By this means, the old shift register bit for that output stage is inverted, if a fault has been detected. Thus, by reading the actual content of the shift register and comparing it with the byte, which has previously been written into it, a channel selective diagnostic information can be derived, e.g. “open load at output stage no. 5”. Table 7 gives a truth table for this.

A dedicated detector logic in each output stage evaluates the control bit and the comparator output level of that stage and provides the signals “sc” in case of short circuit load and “ol” in case of open load. The “sc” and “ol” of all output stages are linked with the status outputs. Table 7 shows, that STATSC or STATOL deliver a logic 0, if a short circuit load or open load have been detected at any output stage. Otherwise, the status outputs are at logic 1. STATSC delivers also a logic 0, if emergency temperature shutdown (ETs) has occurred due to a “soft” short circuit load or overload.

Fig. 12 shows, that the status outputs can only go to low-level, i.e. indicate a fault, if SIE is at logic 1. Thus, the status outputs are disabled during a byte transfer, until SIE is pulled to logic 1 at the end of the transfer. To avoid an erroneous status message due to a switching event at a load output, the enabling of the status outputs is delayed for about 100 µsec.

The timing for parallel loading of fault information into the shift register is also determined by SIE, as shown in fig. 12: As parallel loading is only enabled for SIE at logic 0 level, the fault information is loaded at the beginning of an SPI byte transfer.

OLSD CONDITION AT OUTPUT N			DIAGNOSTIC SIGNALS			
Load Condition	Output State	Vout	Shift Register Bit for Output n		STATOL	STATSC
			Old	New		
"Normal"	off	> V_{ref}	0	0	1	1
	on	< V_{ref}	1	1		
"Open load"	**off**	< V_{ref}	**0**	**1**	**0**	1
	on	< V_{ref}	1	1	1	
"Short circuit load"	off	> V_{ref}	0	0	1	1
	on	> V_{ref}	**1**	**0**		**0**
"Soft short circuit load"	off	> V_{ref}	0	0	1	1
	on	< V_{ref}	1	1		
	off due to emergency temperature shutdown (see section 3.2.2)	> V_{ref}	1	0	1	**0**

Table 7 Diagnostic truth table

(1 = high-level, 0 = low-level; shaded cells indicate signals in case of fault detection)

6.2 Diagnostics with TJA1010 and Microcontroller

The TJA1010 reports diagnostic information to the microcontroller by its status outputs and serial output SO. The easiest way to achieve non channel selective diagnostic information (i.e. open load or short circuit at any output stage), is to read the required status output (STATOL, STATSC), as shown in fig. 13. This can be done by polling the status output from a port pin or by connecting the status output to an interrupt input of the microcontroller. If no distinction between open load and short circuit is required, both status outputs can be parallelled, thus forming a wired-or connection due to their open collector characteristic.

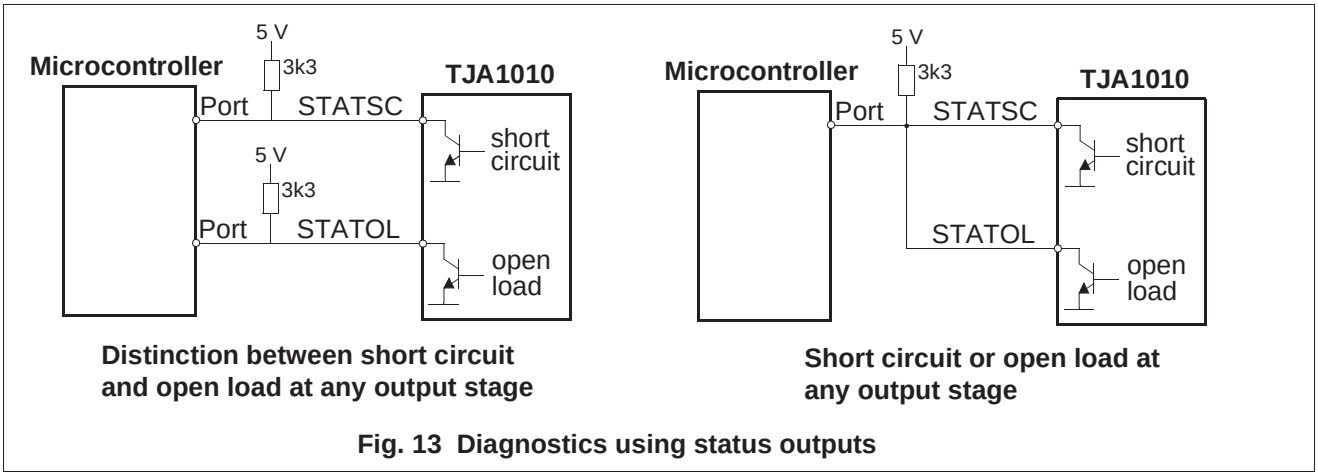

Fig. 13 Diagnostics using status outputs

Channel selective diagnostic information can be derived by evaluating the serial output data of the TJA1010 with the microcontroller. For this purpose, the actual data received from the TJA1010 (new bits) have to be compared with those previously sent to the TJA1010 (old bits). Table 7 shows, that a fault detection at a certain output stage is indicated, if the old and new bit at the respective position are unequal. Otherwise, no fault has been detected.

The flow chart in fig. 14 shows a diagnostic routine, which will find and localize an open load or short circuit load at any output of the TJA1010. Note, that open loads can only be detected in off-state and short circuit loads can only be detected in on-state. Therefore, all output stages are turned off by the first test byte to detect any open loads and then turned on to detect any short circuit loads. The diagnostic information then can be derived by comparing the respective test byte with the byte received from the TJA1010´s SO pin during the following transfer.

Note, that the SIE pin has to be released to logic 1 after transmission of each test byte. This is in order to write the transferred byte into the 8 bit latch for controlling the output stages and allow the diagnostic circuits to invert shift register bits, if failures have been detected.

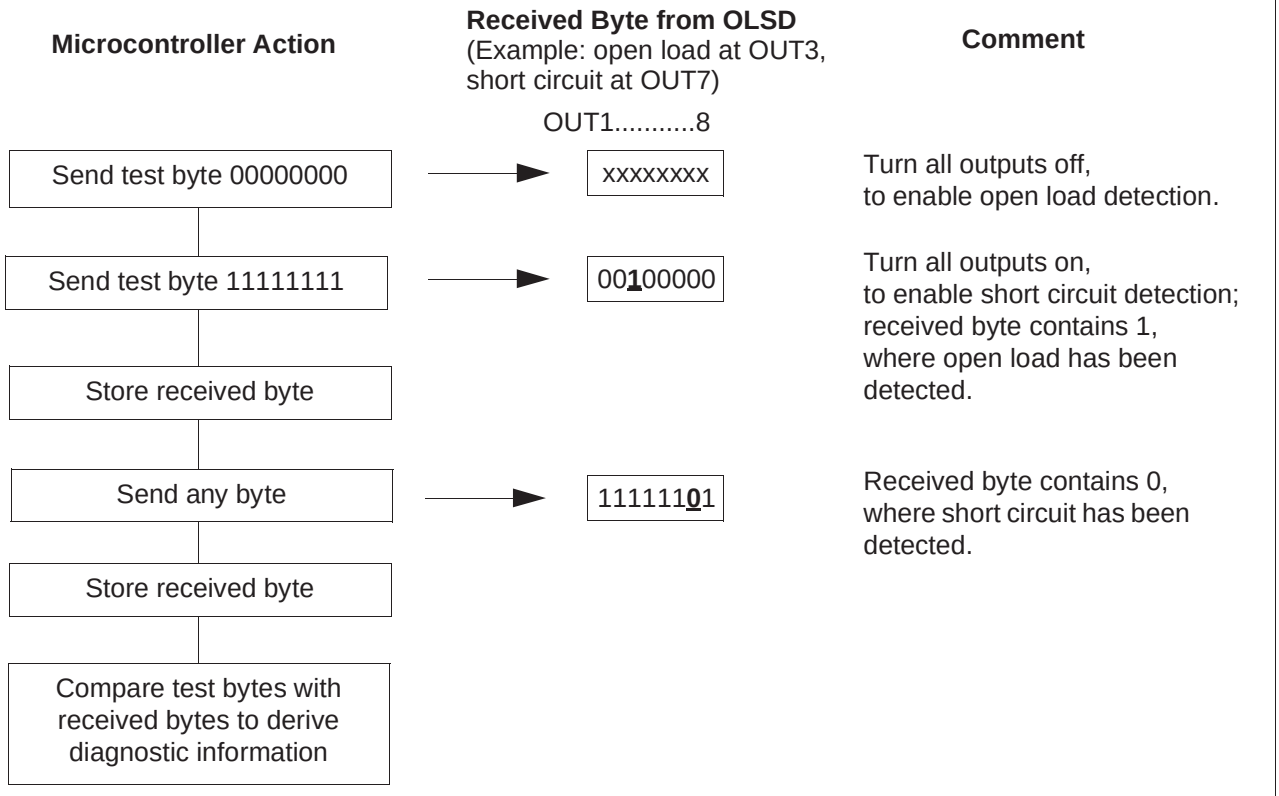

Fig. 14 Diagnostic routine
(1 = high-level, 0 = low-level, x = don't care)

If any short circuit condition has been detected, the respective output stages or - in case of emergency temperature shutdown - all output stages should be turned off until the failure has been removed. Otherwise, the operation of the device at one of the two temperature protection levels over a long time would reduce its reliability.

7. MISCELLANEOUS

7.1 Low-Power Mode

A low-power mode is implemented into the TJA1010, that minimizes the current drawn by the device, and therefore allows to connect it permanently to a car battery. This mode is entered by pulling the stand-by input STBY to low-level. Note, that the minimization of battery current is not only achieved by reducing the supply current flowing into the Vdd-pin. All inputs and outputs are set to a high-ohmic state in low-power mode. The currents at all pins in low-power mode are given in the data sheet.

7.2 Reset

The TJA1010 can be reset by a microcontroller by pulling its stand-by input (STBY) to low-level. This will turn all output stages off. After pulling the stand-by pin again to high-level, this state remains, until new control data are transferred via the SPI interface.

The TJA1010 also has a power-on reset function, i.e. all output stages turn off, if Vdd falls below the undervoltage threshold level of max. 4.3 V. The off-state remains, if Vdd rises above 4.3 V again.

8. REFERENCE

[1] Data Sheet: TJA1010 Octal Low Side Driver (OLSD), Philips Semiconductors (Feb 09, 1998)